THE INVENTION CLAIMED IS:

1. A method comprising:

receiving a circuit design having a plurality of latches; and

allowing one or more latches of the circuit design to be locally treated as exhibiting latch transparency during modeling of the timing behavior of the circuit design.

2. The method of claim 1 wherein receiving the circuit design having a plurality of latches comprises receiving a list of components and connections to the components included in an integrated circuit (IC).

3. The method of claim 1 wherein allowing one or more latches of the circuit design to be locally treated as exhibiting latch transparency during modeling of the timing behavior of the circuit design comprises:

associating a delay with one or more latches coupled to a local clock buffer (LCB) in the circuit design; and

changing a timing model for the one or more latches thereby changing a timing model for the circuit design based on the delay.

4. The method of claim 3 wherein associating a delay with one or more latches includes receiving a user specified delay.

5. The method of claim 3 wherein associating a delay with one or more latches includes delaying a launch clock signal generated by the LCB to at least one of the one or more latches.

6. The method of claim 1 wherein allowing one or more latches of the circuit design to be locally treated as exhibiting latch transparency during modeling of the timing behavior of the circuit design comprises:

determining a list of components and connections to the components included in an integrated circuit (IC);

identifying one or more local clock buffers (LCBs) in the IC;

identifying one or more clock signals of each LCB in the IC;

identifying one or more latches in the IC;

identifying one or more latches coupled to each LCB in the IC;

associating a delay with a local clock coupled to one or more latches in the IC; and

changing a timing model for the one or more latches thereby changing a timing model for the IC based on the delay.

7. A method for modeling latch transparency at a local level comprising:

determining a list of components and connections to the components included in an integrated circuit (IC);

identifying one or more local clock buffers (LCBs) in the IC;

identifying one or more clock signals of each LCB in the IC;

identifying one or more latches in the IC;

identifying one or more latches coupled to each LCB in the IC;

associating a delay with a local clock coupled to one or more latches in the IC; and

changing a timing model for the one or more latches thereby changing a timing model for the IC based on the delay.

8. The method of claim 7 wherein the list of components and connections to the components of the integrated circuit (IC) includes a netlist.

9. The method of claim 7 wherein identifying one or more LCBs in the IC includes employing a first pattern to identify one or more LCBs in the IC.

10. The method of claim 7 wherein identifying one or more clock signals of each LCB in the IC includes employing a first pattern to identify one or more clock signals of each LCB in the IC.

11. The method of claim 7 wherein identifying one or more latches in the IC includes employing a second pattern to identify one or more latches in the IC.

12. The method of claim 7 wherein associating the delay with the local clock includes receiving a user specified delay.

13. The method of claim 7 wherein associating the delay with the local clock includes receiving the delay in a file from the timing tool.

14. The method of claim 7 wherein associating the delay with the local clock includes delaying a launch clock

signal generated by the LCB to at least one of the one or more latches.

15. The method of claim 7 wherein changing the timing model for the one or more latches thereby changing a timing for the IC includes at least one of changing a setup time for a latch in the IC, increasing a delay through the latch, and reducing a clock pulsewidth applied to the latch.

16. The method of claim 7 further comprising including the IC with the changed timing model in a list of ICs and connections to the ICs of a circuit design on which a timing run will be performed.

17. The method of claim 7 further comprising performing a timing run on the timing model of the IC.

18. A computer program product comprising:

a medium readable by a computer, the computer readable medium having computer program code adapted to:

receive a circuit design having a plurality of latches; and

allow one or more latches of the circuit design to be locally treated as exhibiting latch transparency during modeling of the timing behavior of the circuit design.

19. A computer program product comprising:

a medium readable by a computer, the computer readable medium having computer program code adapted to:

determine a list of components and connections to the components of an integrated circuit (IC);

identify one or more local clock buffers (LCBs) in the IC;

identify one or more clock signals of each LCB in the IC;

identify one or more latches in the IC;

identify one or more latches coupled to each LCB in the IC;

associate a delay with a local clock coupled to one or more latches in the IC; and

change a timing model for the one or more latches thereby changing a timing model for the IC based on the delay.